



PTO/SB/08A (08-03)

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1

of 5

**Complete if Known**

Application Number	10/762,181
Filing Date	January 21, 2004
First Named Inventor	Mohklesi
Art Unit	
Examiner Name	
Attorney Docket Number	SAND-01021US0

**U. S. PATENT DOCUMENTS**

Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
		US- 5,043,940	8/27/1991	Harari	
		US- 5,095,344	3/10/1992	Harari	
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		US- 6,121,654	9/19/2000	Likharev	
		US- 6,151,248	11/21/2000	Harari et al.	

**FOREIGN PATENT DOCUMENTS**

Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>6</sup>
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		Filing Date	January 21, 2004
		First Named Inventor	Mohklesi
		Art Unit	
		Examiner Name	
Sheet 3	of 4	Attorney Docket Number	SAND-01021US0

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	1	BORSON, et al., "Direct Measurement of the Energy Distribution of Hot Electrons in Silicon Dioxide," J. Appl. Phys., Vol. 58, No. 3.1, August 1985, pp. 1302-1313	
	2	BROWN, et al., "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide to Understanding and Using NVSM Devices," IEEE, pp. 198-200	
	3	CAMM, et al., "Engineering Ultra-Shallow Junctions Using rRTP™," IEEE, Vortek Industries Limited, 2002	
	4	CHAN, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," IEEE Electron Device Letters, Vol. EDL-8, No. 3, March 1987, pp. 93-95	
	5	CHOI, et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling-Down and Zero Program Disturbance," IEEE Symposium on VLSI Technology Digest of Technical Papers, 1996, pp. 238-239	
	6	CHOI, et al., "A Triple Polysilicon Stacked Flash Memory Cell With Wordline Self-Boosting Programming", IEEE, 1997, pp. 283-286	
	7	DIJKSTRA, et al., "ISSG RTO (In-situ Steam Generation Rapid Thermal Oxidation) Grown Tunnel Oxide for Improved Reliability of Flash Memories," Philips Semiconductors, pp. 85-86	
	8	DiMARIA, "Graded or Stepped Energy Band-Gap-Insulator MIS Structures (GI-MIS or SI-MIS)," American Institute of Physics, September 1979, pp. 5826-5828	
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	10	DiMARIA, et al., "Electrically-Alterable Memory Using A Dual Electron Injector Structure," IEEE Electron Device Letters, Vol. EDL-1, No. 9, September 1980, pp. 179-180	

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		DiMARIA, et al., "Extended Cyclability in Electrically-Alterable Read-Only-Memories," IEEE ELECTRON DEVICE LETTERS, VOL. EDL-3, NO. 7, July 1982, pp. 191-195	
		HIRAYAMA, et al., "Low-Temperature Growth of High-Integrity Silicon Oxide Films by Oxygen Radical Generated in High-Density Krypton Plasma," IEEE, 1999, pp. 10.3.1-10.3.4	
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		OHTSUBO, et al., "Low Temperature Growth (400°C) of High-Integrity Thin Silicon-Oxynitride Films by Microwave-Excited high-Density Kr/O <sub>2</sub> /NH <sub>3</sub> Plasma," pp. 166-169	

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		SATOH, et al., "A Novel Channel Boost Capacitance (CBC) Cell Technology with Low Program Disturbance Suitable for Fast Programming 4Gbit NAND Flash Memories", IEEE Symposium on VLSI Technology Digest of Technical Papers, 1998, pp. 108-109	
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		SEIDEL, et al., "Progress and Challenges for ALD Applications," Genus, Inc., August 5, 2003, pp. 1-39	
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		YU, et al., "Energy gap and band alignment for (HfO <sub>2</sub> )x(Al <sub>2</sub> O <sub>3</sub> )1-x on (100) Si," Applied Physics Letters, Volume 81, Number 2, July 8, 2002, pp. 376-378	

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